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1 Simulation-based verification using Temporally Attributed Boolean Logic

S. K. Panda, Arnab Roy, P. P. Chakrabarti, Rajeev Kumar
September 2008 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 13 Issue 4
Publisher: ACM
Full text available: Pdf (1.49 MB) Additional Information: full citation, abstract, references, index terms
Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 5, Citation Count: 0

We propose a specification logic called Temporally Attributed Boolean (TAB) Logic for Assertion Based Verification, which allows us to: (i) represent assertions succinctly, (ii) incorporate data-orientation and (iii) associate timing to design intentions. ...

Keywords: Bus verification, instruction semantics verification, interrupt testing, offline-online verification algorithm, simulation based verification, temporal logic, timing verification

2 Fault tolerant bus architecture for deep submicron based processors

N. Venkateswaran, S. Balaji, V. Sridhar
March 2005 ACM SIGARCH Computer Architecture News, Volume 33 Issue 1
Publisher: ACM

Full text available: Pdf (407.42 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 37, Citation Count: 0

In the Deep Submicron era testing of processors is gaining prominence due to the effect of many analog faults. These faults have a direct impact on the signal integrity in interconnects. In deep submicron based processors electromigration poses a major ...

Keywords: deep submicron technology, electromigration, fault tolerance, interconnect

3 Fundamentals of fault-tolerant distributed computing in asynchronous environments

Felix C. Gärtner
March 1999 ACM Computing Surveys (CSUR), Volume 31 Issue 1
Publisher: ACM

Full text available: Pdf (203.96 KB) Additional Information: full citation, abstract, references, cited by, index terms, review

Bibliometrics: Downloads (6 Weeks): 37, Downloads (12 Months): 390, Citation Count: 14

Fault tolerance in distributed computing is a wide area with a significant body of literature that is vastly diverse in methodology and terminology. This paper aims at structuring the area and thus guiding readers into this interesting field. We use ...

Keywords: agreement problem, asynchronous system, consensus problem, failure correction, failure detection, fault models, fault tolerance, liveness, message passing, possibility detection, predicate detection, redundancy, safety

4 Software-controlled fault tolerance

George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August, Shubhendu S. Mukherjee
December 2005 ACM Transactions on Architecture and Code Optimization (TACO), Volume 2 Issue 4
Publisher: ACM

Full text available: Pdf (638.90 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 227, Citation Count: 4

Traditional fault-tolerance techniques typically utilize resources ineffectively because they cannot adapt to the changing reliability and performance demands of a system. This paper proposes software-controlled fault tolerance, a concept allowing designers ...

Keywords: Software-controlled fault tolerance, fault detection, reliability

5 Concurrent fault detection for a multiple-plane packet switch

Roberto Rojas-Cessa, Eiji Oki, H. Jonathan Chao
August 2003 IEEE/ ACM Transactions on Networking (TON), Volume 11 Issue 4
Publisher: IEEE Press
Full text available: Pdf (711.66 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 38, Citation Count: 0

In high-speed and high-capacity packet switches, system reliability is critical to avoid loss of huge amounts of information and retransmission of traffic. We propose a series of concurrent fault-detection mechanisms for a multiple-plane crossbar-based ...

Keywords: concurrent testing, fault detection, packet switch, parallel planes, single fault

6 Fault Tolerance Techniques for the Merrimac Streaming Supercomputer

Mattan Erez, Nuwan Jayasena, Timothy J. Knight, William J. Dally
November 2005 SC '05: Proceedings of the 2005 ACM/IEEE conference on Supercomputing
Publisher: IEEE Computer Society
Full text available: Pdf (355.23 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 57, Citation Count: 0

As device scales shrink, higher transistor counts are available while soft-errors, even in logic, become a major concern. A new class of architectures, such as Merrimac and the IBM Cell, take advantage of the higher transistor count by exposing control, ...

7 Transient-fault recovery for chip multiprocessors

Mohamed Gomaa, Chad Scarbrough, T. N. Vijaykumar, Irith Pomeranz
May 2003 ACM SIGARCH Computer Architecture News, Volume 31 Issue 2
Publisher: ACM

Full text available: Pdf (370.75 KB) Additional Information: full citation, abstract, references, cited by

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 52, Citation Count: 35

To address the increasing susceptibility of commodity chip multiprocessors (CMPs) to transient faults, we propose Chiplevel Redundantly Threaded multiprocessor with Recovery (CRTR). CRTR extends the previously-proposed CRT for transient-fault detection ...

8 Transient-fault recovery for chip multiprocessors

Mohamed Gomaa, Chad Scarbrough, T. N. Vijaykumar, Irith Pomeranz
June 2003 ISCA '03: Proceedings of the 30th annual international symposium on Computer architecture
Publisher: ACM

Full text available: Pdf (370.75 KB) Additional Information: full citation, abstract, references, cited by

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 52, Citation Count: 35

To address the increasing susceptibility of commodity chip multiprocessors (CMPs) to transient faults, we propose Chiplevel Redundantly Threaded multiprocessor with Recovery (CRTR). CRTR extends the previously-proposed CRT for transient-fault detection ...

9 Transient fault detection via simultaneous multithreading

Steven K. Reinhardt, Shubhendu S. Mukherjee
May 2000 ACM SIGARCH Computer Architecture News, Volume 28 Issue 2
Publisher: ACM

Full text available: Pdf (151.56 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 112, Citation Count: 59

Smaller feature sizes, reduced voltage levels, higher transistor counts, and reduced noise margins make future generations of microprocessors increasingly prone to transient hardware faults. Most commercial fault-tolerant computers use fully ...

10 Transient fault detection via simultaneous multithreading

Steven K. Reinhardt, Shubhendu S. Mukherjee
June 2000 ISCA '00: Proceedings of the 27th annual international symposium on Computer architecture
Publisher: ACM

Full text available: Pdf (151.56 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 112, Citation Count: 59

Smaller feature sizes, reduced voltage levels, higher transistor counts, and reduced noise margins make future generations of microprocessors increasingly prone to transient hardware faults. Most commercial fault-tolerant computers use fully ...

11 SWIFT: Software Implemented Fault Tolerance

George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August
March 2005 CGO '05: Proceedings of the international symposium on Code generation and optimization
Publisher: IEEE Computer Society

Full text available: Pdf (214.08 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 64, Citation Count: 21

To improve performance and reduce power, processor designers employ advances that shrink feature sizes, lower voltage levels, reduce noise margins, and increase clock rates. However, these advances make processors more susceptible to transient faults ...

12 Efficient on-line testing of FPGAs with provable diagnosabilities

Vinay Verma, Shantanu Dutt, Vishal Suthar
June 2004 DAC '04: Proceedings of the 41st annual conference on Design automation
Publisher: ACM

Full text available: Pdf (335.66 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 20, Citation Count: 2

We present novel and efficient methods for on-line testing in FPGAs. The testing approach uses a ROving TEster (ROTE), which has provable diagnosabilities and is also faster than prior FPGA testing methods. We present 1- and 2-diagnosable built-in self-tester ...

Keywords: FPGAs, built-in self-tester (BISTer), diagnosability, functional testing, on-line testing, roving tester (ROTE)

13 SEU tolerant device, circuit and processor design

William Heidergott
June 2005 DAC '05: Proceedings of the 42nd annual conference on Design automation
Publisher: ACM
Full text available: Pdf (364.56 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 117, Citation Count: 1

Development of highly reliable and available systems requires consideration of the occurrence of single event upsets, the effects they have on system ...

Keywords: error detection and correction coding, fault avoidance, fault masking, fault tolerant systems, modular redundancy, radiation effects, single event upset, soft error rate, temporal redundancy

14 Self-calibrating Online Wearout Detection

Jason Blome, Shuguang Feng, Shantanu Gupta, Scott Mahlke
December 2007 MICRO '07: Proceedings of the 40th Annual IEEE/ACM International Symposium on Microarchitecture
Publisher: IEEE Computer Society
Full text available: Pdf (551.92 KB) Additional Information: full citation, abstract, index terms

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 67, Citation Count: 1

Technology scaling, characterized by decreasing feature size, thin- ning gate oxide, and non-ideal voltage scaling, will become a major hindrance to microprocessor reliability in future technology gener- ations. Physical analysis of device failure mechanisms ...

15 ACM SIGSOFT Software Engineering Notes: Volume 33 Issue 5

August 2008 issue Volume 33 Issue 5
Publisher: ACM
Additional Information: full citation

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation Count: 0

16 Micro embedded monitoring for security in application specific instruction-set processors

Roshan G. Ragel, Sri Parameswaran, Sayed Mohammad Kia
September 2005 CASES '05: Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems
Publisher: ACM

Full text available: Pdf (357.72 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 74, Citation Count: 3

This paper presents a methodology for monitoring security in Application Specific Instruction-set Processors (ASIPs). This is a generalized methodology for inline monitoring insecure operations in machine instructions at microinstruction level. Microinstructions ...

Keywords: application specific instruction-set processors, micro embedded monitoring, microinstructions, security monitoring, self-monitoring instructions

17 Hardware support for code integrity in embedded processors

Milena Milenkovi•, Aleksandar Milenkovi•, Emil Jovanov
September 2005 CASES '05: Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems
Publisher: ACM

Full text available: Pdf (371.76 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 93, Citation Count: 1

Computer security becomes increasingly important with continual growth of the number of interconnected computing platforms. Moreover, as capabilities of embedded processors increase, the applications running on these systems also grow in size and complexity, ...

Keywords: attacks, code injection, code integrity

18 EBIST: A Novel Test Generator with Built-In Fault Detection Capability

Dhiraj K. Pradhan, Chunsheng Liu, Krish Chakraborty
March 2003 DATE '03: Proceedings of the conference on Design, Automation and Test in Europe - Volume 1, Volume 1
Publisher: IEEE Computer Society

Full text available: Publisher Site, Pdf (166.62 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 5, Citation Count: 0

A novel design methodology for test pattern generation in BIST is presented. Here faults and errors in the generator itself are detected. Two different design methodologies are presented. The first one guarantees all single fault/error detection and ...

19 Fault-tolerance in FPGA's through CRC voting

Helano Castro, Alexandre Augusto Coelho, Ricardo Jardel Silveira

September 2008 SBCCI '08: Proceedings of the twenty-first annual symposium on Integrated circuits and system design

Publisher: ACM

Full text available: Pdf (386.63 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 6, Citation Count: 0

The use of FPGA's for implementing fault-tolerant systems (FTS) has been widely discussed. Many FTS's have been proposed in this context and TMR is by far the most used architecture. However, those implementations have to count on the memory configuration's ...

Keywords: FPGA, cyclic redundancy check, fault tolerance, partial reconfiguration

20 A probabilistic reasoning framework for smart homes

Todor Dimitrov, Josef Pauli, Edwin Naroska

November 2007 MPAC '07: Proceedings of the 5th international workshop on Middleware for pervasive and ad-hoc computing: held at the ACM/IFIP/USENIX 8th International Middleware Conference

Publisher: ACM

Full text available: Pdf (975.11 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 38, Citation Count: 0

Inference and reasoning in modern AmI (Ambient Intelligence) middlewares is still a complex task. Currently no common patterns for building smart applications can be identified. This paper presents an ongoing effort to build a generic probabilistic reasoning ...

Keywords: Bayesian inference, ambient intelligence, man-in-the-loop analysis, pervasive computing, probabilistic reasoning

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